Pag 4

Detail d Description

Figures 1 through 6 are a sequence of sectional views through a semiconductor substrate illustrating the steps in the method of fabricating a Schottky diode ~~20~~ in accordance with the invention, with Figures 6 and 7 illustrating the resultant Schottky diode. While the Schottky diode ~~20~~ is typically fabricated as a part of an integrated circuit, the Schottky diode ~~20~~ may be fabricated as a discrete component.

PAGE 5:

As shown in Figure 1, an active area 22 in which a Schottky diode ~~20~~ will be fabricated is developed in semiconductor substrate 24 of one conductivity type, i.e. either p-type or n-type. Semiconductor substrate 24 in a preferred embodiment is silicon, but the invention is not limited thereto. Other known semiconductor substrates, including but not limited to germanium and group III-IV compounds, may be used. The size and shape of active area 22 is dependent on the Schottky diode to be fabricated therein.

Oxide may be removed from the initial upper surface 26 of semiconductor substrate 24 such as by an etch step, as is known in the art. Not required by the invention, but when the Schottky diode ~~20~~ is fabricated as part of an existing process to produce bipolar transistors, a dopant of a conductivity type opposite to the conductivity type of semiconductor substrate 24 is implanted over active area 22 to form a buried layer 28. An example will be described herein in which semiconductor substrate 24 is silicon of p-type conductivity and the implanted dopant is n-type such as phosphorus, arsenic, or antimony, but the invention is not limited thereto. Subsequent to the implant step, an epitaxial layer 30 of substrate material is grown of at least a sufficient thickness to meet breakdown requirements of the integrated circuit in which the Schottky diode ~~20~~ is fabricated. The upper surface of layer 30 defines surface 32 at this point in the process. Epitaxial layer 30 becomes part of semiconductor substrate 30. In the illustrated embodiment, the epitaxial layer 30 is approximately 12,000 angstroms thick, defines surface 32 as mentioned above, and is grown by any suitable known process.

Buried layer 28 formed beneath the initial upper surface 26 of semiconductor substrate 24 may diffuse into the lower portion of epitaxial layer 30.

Electrical isolation regions 36, 38, and 40 are formed by known techniques, including, but not limited to LOCOS, recessed or non-recessed poly-buffered LOCOS, shallow trench

PAGE 7:

Additional layers of electrical insulating material may be applied. In the illustrated embodiment, a third layer 74 of phosphorus doped oxide (PTEOS) is applied over layer 72 and is applied by a plasma enhanced chemical vapor deposition (PECVD) process. Layer 74 may be 2000 angstroms thick.

A fourth layer of electrical insulating material may be applied. In the illustrated embodiment, a fourth layer 76 of boron and phosphorus doped oxide is applied over layer 74 in a blanket deposition. Layer 76 may be thicker than layer 72 and is applied by a PECVD process. Layer 76 may be 3000 angstroms thick.

As illustrated in Figure 3, photoresist 78 is patterned on the uppermost layer of electrical insulating material with an aperture 80 over area 52 in preparation of etching a window.

As illustrated in Figure 4, window 82 is etched through the layers of electrical insulating material 70 and 72, as well as any other layers present such as layers 74 and 76 in the illustrated embodiment. Window 82 may be etched by any known process such as by an aqueous solution containing hydrogen fluoride or a plasma etching process with an etchant for the particular insulating materials used in the layers. Window 82 extends at least to surface 32 defining an area 52 of semiconductor substrate 24 where the semiconductor substrate is exposed due to the etch, and where the metal-semiconductor junction of the Schottky diode ~~20~~ will be formed. Area 52 is less than the area of aperture 80 in photoresist 78. The etching solutions or plasma etching conditions and the specific electrical insulating materials are chosen to have different etching rates of the various layers of insulating material. As the etching of

window 82 proceeds, the differences in etching rates provide shaping of side walls 54 of window 82 to define the final structure of window 82 at the conclusion of the etching step. The top layer of insulative material typically has an etching rate that is the same as or higher, that is etches away

PAGE 9:

treatm nt causes the silicide forming metal to react with substrate 24 in area 52 to form silicide 84 illustrated in Figure 5. Subsequently, the unreacted metal is etched away. The silicide is a transition metal that provides the function of defining the Schottky barrier and thus some of the characteristics of the diode.

One or more barrier layers 88 may be employed. In the illustrated embodiment, a barrier layer of titanium nitride is shown in Figure 6. Although the barrier layer 88 of titanium nitride is not shown as extending along the side walls 54 of window 82, the invention is not so limited. Titanium nitride may be deposited by a sputtering process.

A metal layer of any known metal which will provide both a contact to the rectifying junction with the semiconductor material of semiconductor substrate 24 and its associated field plate is deposited. By way of example and not limitation, if the semiconductor substrate 24 is silicon, the metal layer may be aluminum, chromium, or rhodium; if the semiconductor substrate 24 is germanium, the metal layer may be of gold or chromium, and if the semiconductor substrate 24 is a group III - V semiconductor compound, such as gallium arsenide, the metal layer may be aluminum or gold. In the illustrated embodiment, aluminum is deposited by a sputtering deposition process.

The layer of metal (not shown) is patterned and etched to remove metal from areas where metal is not desired. A portion of the layer of metal that remains forms traces to conduct electrical energy to or from the Schottky diode ~~20~~. Metal 86, which forms part of the Schottky diode ~~20~~, remains completing the Schottky diode ~~20~~. One or

more subsequent steps may occur. For example, a hydrogen bake may be used to passivate the surface.

Alternately, a silicide may be deposited, or a metal layer of any known metal which will provide a surface barrier rectifying junction with the semiconductor material of substrate 24

PAGE 11:

topography of the side walls 54 of window 82 of the first and second layers of insulative material is achieved in a single etch step as a result of second layer of insulative material 72 having a greater etch rate than the etch rate of first layer of insulative material 70. Depending on the relative etching rates of insulative material in the various layers, a step 94 can selectively be achieved at the interface of layers 70 and 72, at the interface of layers 72 and 74, or at the interface of layers 74 and 76.

In the illustrated embodiment, the width 96 of extended portion 100 forming step 94 of the first layer of insulative material is approximately 1000 angstroms, and concomitantly, metal 86 over extended portion 100 is also approximately 1000 angstroms. The length of width 96 is of sufficient size or dimension relative to the height 98 to overcome short channel effects of extended portion 100 in conjunction with metal 86 and substrate 24 operating as a MOS device. It is not the dimensions of extended portion 100, by themselves, that are important. Rather a resulting structure 102, of metal 86 on step 94 separated from substrate 24 by an insulating material, forming and functioning as an MOS device such that when the Schottky diode ~~20~~ is reverse biased, the stepped structure, which is a metal oxide semiconductor depletes or inverts the silicon region 92 beneath step 94, depending on the surface conditions, the thin insulative layer region of extended portion 100, and the bias applied, thereby controlling pinching and cornering effects in the depletion region. As a result, the Schottky diode ~~20~~ has very low leakage reverse bias characteristics, and breakdown of the Schottky diode ~~20~~ occurs when the reverse bias exceeds the breakdown of the insulative material.

While the invention has not been described as being useful with a guard ring, use of a guard ring with the Schottky diode ~~20~~ is contemplated within the scope of the invention.